Patent Application

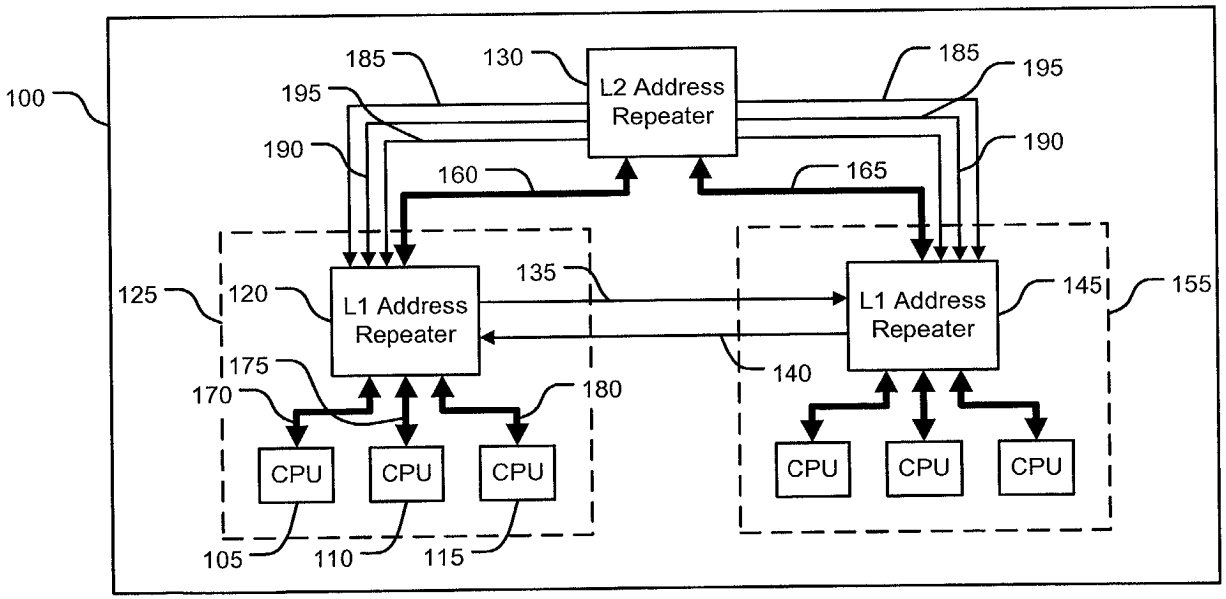

Figure 1

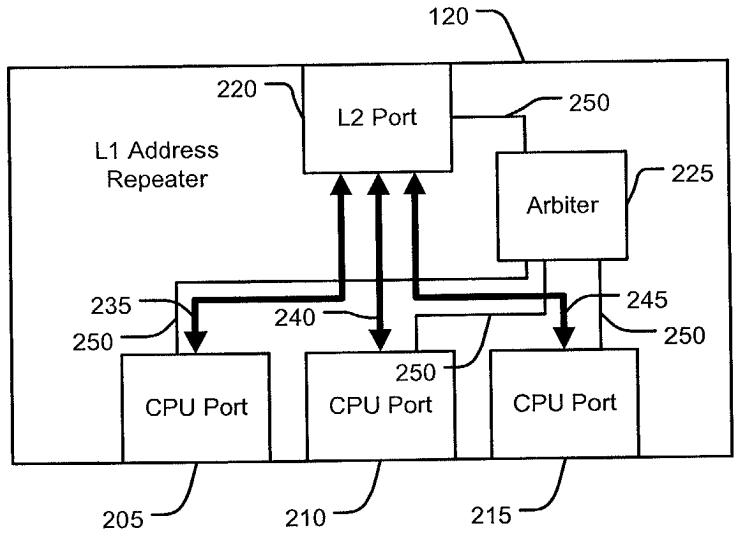

Figure 2

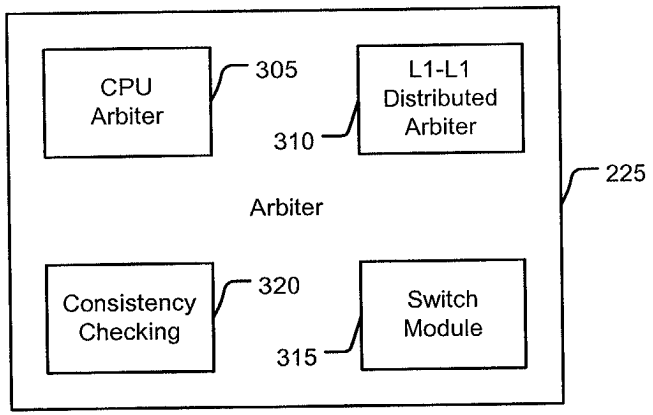

Figure 3

PATENT PENDING

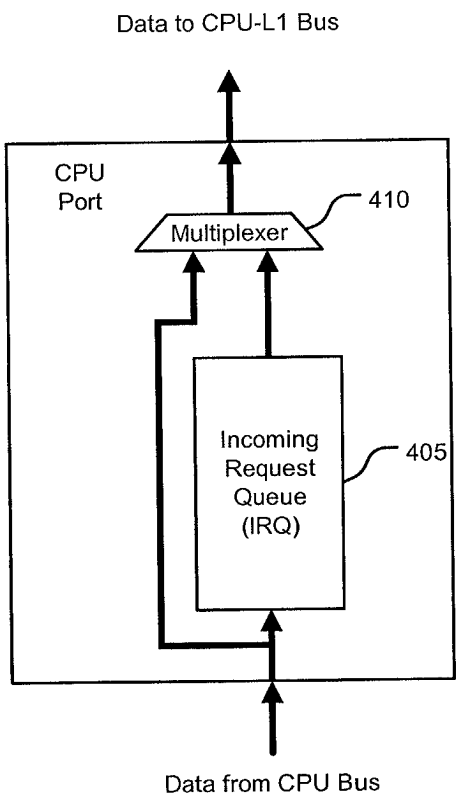

Figure 4(a)

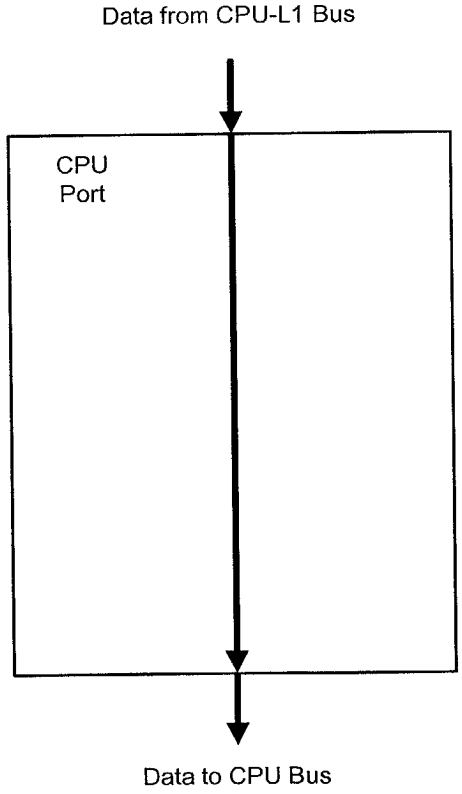

Figure 4(b)

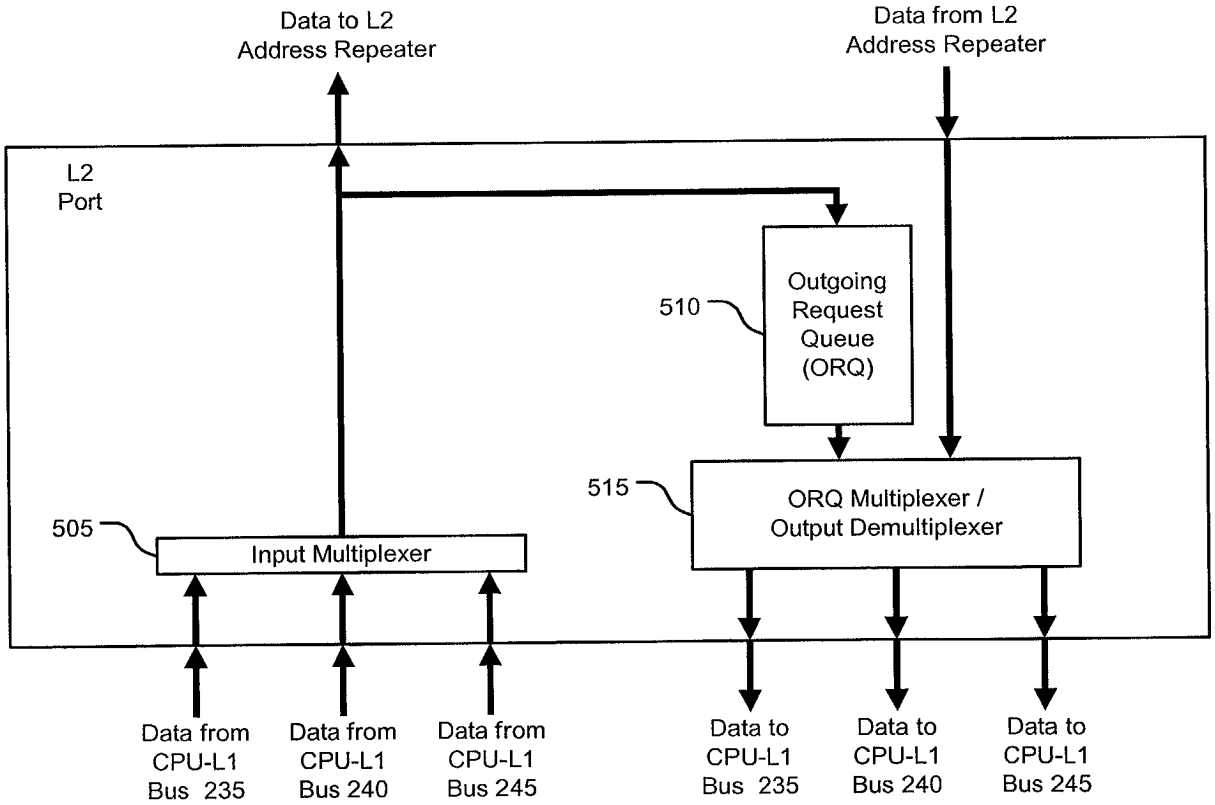
Data to L2
Address Repeater
Data from L2
Address Repeater
L2
Port
Outgoing
Request
Queue
(ORQ)
510
515
ORQ Multiplexer /
Output Demultiplexer
505
Input Multiplexer
Data from
CPU-L1
Bus 235
Data from
CPU-L1
Bus 240
Data from
CPU-L1
Bus 245
Data to
CPU-L1
Bus 235
Data to
CPU-L1
Bus 240
Data to
CPU-L1
Bus 245

Figure 5

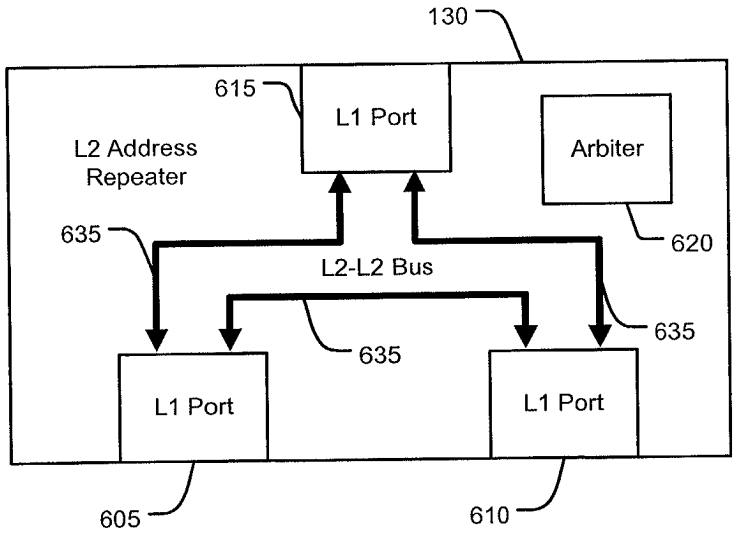
130
615
L1 Port
L2 Address
Repeater
Arbiter
620
635
L2-L2 Bus
635
635
L1 Port
L1 Port
605
610

Figure 6

PATENT CLOSED

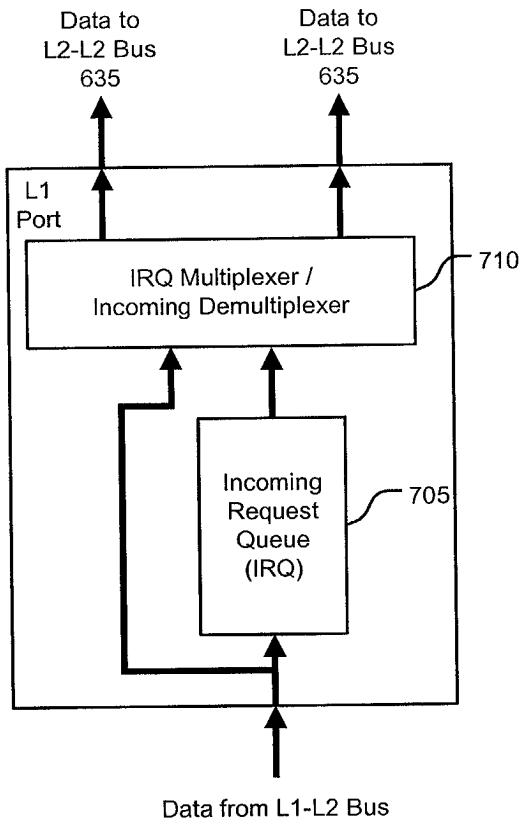

Figure 7(a)

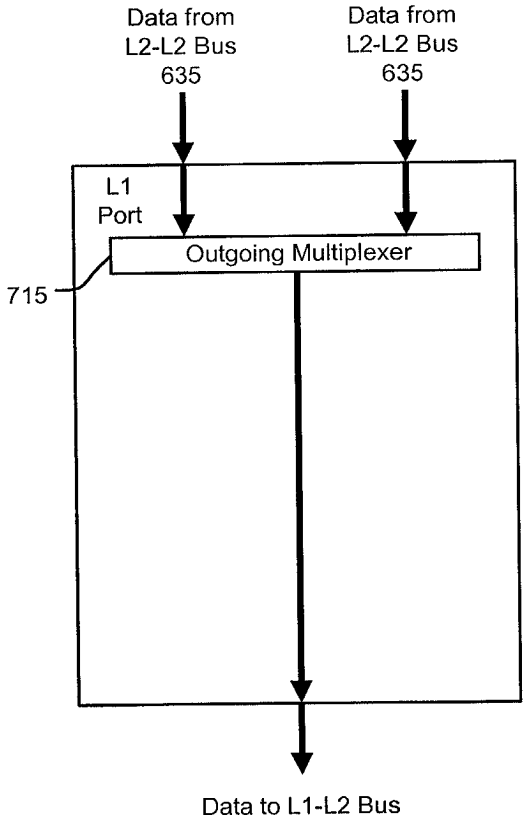

Figure 7(b)

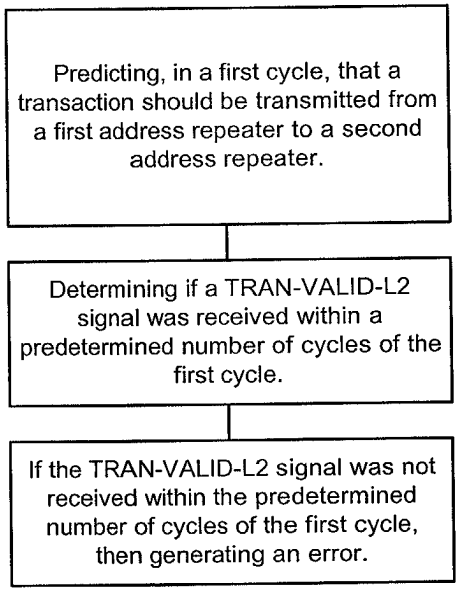

Figure 8(a)

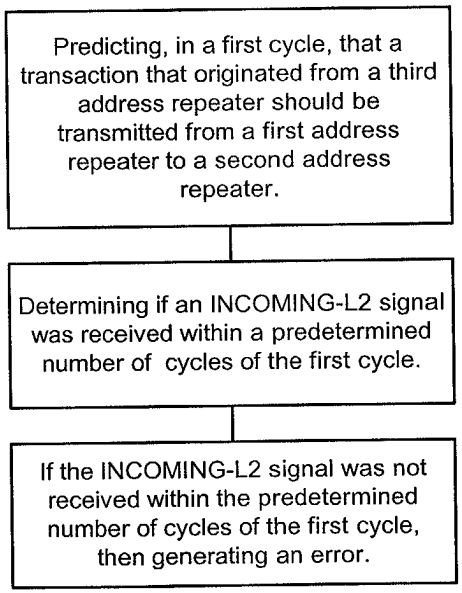

Figure 8(b)

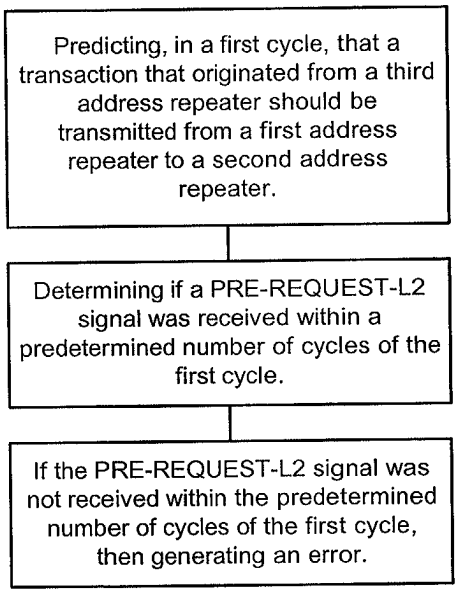

Figure 8(c)

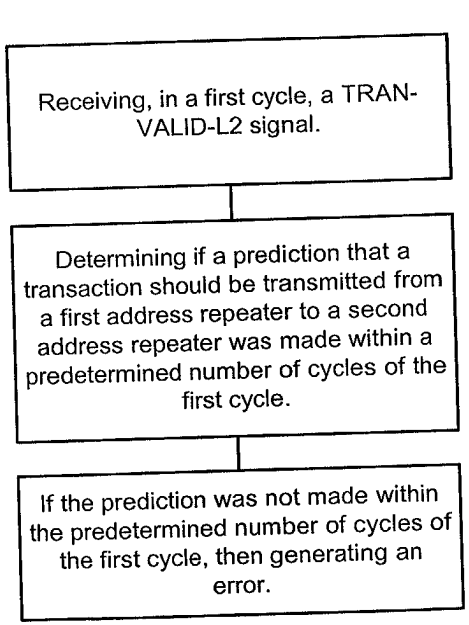

Figure 9(a)

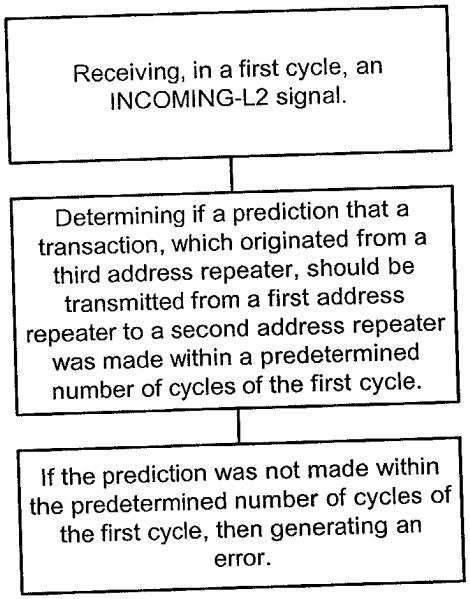

Figure 9(b)

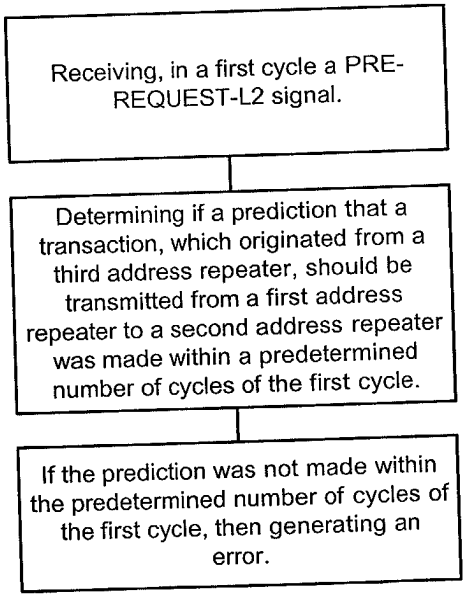

Figure 9(c)